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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,536	12/28/2001	Lyn Mark Elzinga	42390.P13294	9793

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EXAMINER
SIEK, VUTHE

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,536	ELZINGA, LYN MARK	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-18,20-35,37 and 38* is/are rejected.

7)☒ Claim(s) *7,8,19 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 10/040,536 filed on 12/28/2001. Claims 1-38 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 9-18, 20-35 and 37-38 are rejected under 35 U.S.C. 102(b) as being anticipated by DeBrosse et al. (5,534,732).

4. As to claim 1, DeBrosse et al. teach a method comprising swizzling a set of N concurrently active signal lines into a first order to provide a first stage of capacitive noise cancellation of a first plurality of signal lines of the set (crossing region as shown in the Figs. 5, 7, 8, 9, 10 and 11); and swizzling the set of N concurrently active signal lines again into a second order different from the first order to provide a second stage of further capacitive noise cancellation for the first plurality of signal lines of the set (Figs. 5, 12, Figs. 5, 7, 8, 9, 10 and 11 provide first region of parallel signal lines, crossing region of swizzling signal lines, and a third region of different swizzling signal lines (reordered signal lines to restore in3itial ordering as in the first region) in order to eliminate capacitive coupling noise; set of signal lines include subsets can be considered as a first subset, second subset, third subset of signal lines being disjoint; col. 2, lines 36-67; col. 3, lines 1-32; col. 4, line 28 to col. 8, line 14). As shown in Figs.

5, 7, 8, 9, 10 and 11, since each of conductor of signal lines inherently includes inductive and capacitive parasitics, capacitive coupling noise cancellation as taught by DeBrosse et al. would inherently include inductive and coupling noise cancellation. DeBrosse et al. teach swizzling signal lines of integrated circuits (col. 1), thus the signal lines transmitting bits of information in transmission cycle.

5. As to claims 14 and 28, DeBrosse et al. teach an apparatus comprising an interconnection array layout of a set of N signal lines to transmit N bits of information in a transmission cycle (Figs. 5, 7, 8, 9, 10 and 11). The interconnection array layout including three regions: a first region comprising the signal lines being substantially parallel an having a first portion with a first signal line order (shown as in the first region of the figures); a first swizzle stage of the set of N signal lines having a second portion with a second signal line order (shown as in the crossing region of the figures), wherein a first signal line of the set is adjacent to a first set subset of the N signal lines in said first portion and the first signal line is adjacent to a second subset of the N signal lines in said second portion, the first subset and the second subset being disjoint (first subset of the N signal lines in the first region, lines 11 to 33; second subset of the N signal lines in the crossing region, lines 11 to 33; the subsets are disjoint since they are in different regions, for example Fig. 5); and a second swizzle stage of the set of N signal lines having a third portion with a third signal line order (shown as in the second region of the figures), wherein the first signal lines of the set is adjacent to a third subset of the N signal lines in said third portion, the first subset, the second subset and the third subset being disjoint (third subset of the N signal lines in the second region, lines 11 to 33; the

first subset, the second subset and the third subset being disjoint, since they are in different region, see Fig. 5 for example).

6. As to claims 15-18 and 29-35, the set of N signal lines have a substantially common origin and a substantially common destination (For example Fig. 5, original in the first region, destination in the second region); figures 13-15 shown set of N signal lines routing in different regions (portions) are optionally via one or more substantially parallel planar layers, where they are connected by vias; wherein the first swizzle stage of the set of N lines comprising a swizzle cell coupling the first portion with the second portion (shown in the crossing region); wherein the second swizzle stage of the set of N lines comprising a swizzle cell coupling the second portion with the third portion (the crossing region coupling the second region); the third portion of the second swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal line that they are adjacent to in the second portion of the first swizzle stage, wherein the second portion of the first swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the first portion, wherein the third portion of the second swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the first portion (shown in the figures, signal lines in the different regions are not placed adjacent from one another); the second region (third swizzle cell) restore initial order of the set of N signal lines as in the first region. The signal lines in different regions are used to reduce capacitive and inductive noise.

7. As to claim 24, DeBrosse et al. teach an interconnection layout comprising a set of N active signal lines having an initial order (as shown in Fig. 5 for example); means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation (shown in Fig. 5 for example). DeBrosse et al. shown capacitive noise cancellation. Since capacitive and inductive parasitic are inherently included in conductive line, thus capacitive noise cancellation inherently includes inductive noise cancellation.

8. As to claim 37, DeBrosse et al. teach an interconnection layout (apparatus) comprising a set of N concurrently active signal lines, the signal lines being substantially parallel and having an first signal line order (shown in the first region in Fig. 5 for example); a plurality of swizzle cells linking segments of the set of N concurrently active signal lines, the plurality of swizzle cells transposing near victim signal lines and far victim signal lines in subsequent segments to facilitate capacitive and inductive noise cancellation within the set of N concurrently active signal lines (the same crossing region could be placed along the longer signal lines, thus the regions are linked from one to another, victim signal lines are inherently within the interconnection layout, since some signal lines are characterized as aggressive signal lines since they are carried signals and other signal lines are considered as victim signal lines); and an optional swizzle cell to restore an initial order for the set N concurrently active signal lines (the

second region restore an initial order for the set of N signal lines as in the first region, Fig. 5 for example).

9. As to claim 38, the interconnection layout of Fig. 5 is implemented in integrated circuits, where the interconnection layout comprising set of N signal lines that are concurrently active indicating that each of the N signal lines may be switched in a signal transmission cycle (art inherent).

10. As to claims 2, and 12-13, DeBrosse et al. teach swizzling signal lines (set of signal lines including subsets (considered as first, second, third, fourth, subsets in different or same regions depending on how to characterize whether segments of signal lines being in different or same regions) (subsets of (1, 2, $\overline{1}$, $\overline{2}$), (3, 4, $\overline{3}$, $\overline{4}$), ... in the set of signal lines) of the set in Figs. 5, 7, 8, 9, 10 and 11. the swizzling signal lines include a first region, a crossing region, and a second region, wherein a first signal line of the set (set of signal lines as shown in Fig. 5) is adjacent to a first subset of the set of N concurrently active signal lines in the first stage and swizzling the set of N concurrently active signal lines again places the first signal line adjacent to a second subset of the set of N concurrently active signal lines in the second stage, the first and second subsets being disjoint (subsets in first region, crossing region and second region are disjoint). The swizzling signal lines as shown cancel inductive and capacitive noise.

11. As to claims 3-6, 20-23 and 25-27, remarks set forth in claims 2 and 12-13 equally apply to reject claims 3-6, 20-23 and 25-27. It should be noted that swizzling signal lines in the crossing region are reordered in the third region in order to obtain initial signal lines a in the first region or as original signal lines configuration in initial

stage, where the signal lines are substantially parallel (Please see Figs. 5, 7, 8, 9, 10 and 11).

12. As to claims 9-11, the claims are merely article of manufacturing to perform the method claims 6, 3 and 1. Therefore, claims 9-11 are also rejected for the same rationale as to reject claims 6, 3 and 1 above.

Allowable Subject Matter

13. Claims 7-8, 19 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Although the prior art may provide multiple stage S, but the prior art of record does not suggest swizzling N lines to provide S stages, wherein S stages being computed from N signal lines according to equation as defined in the claims.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (703) 305-4958. The examiner can normally be reached on M-F (6:30-4:00) 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Vuthe Siek
Primary Examiner
June 18, 2003